A 0.6μm CMOS, 622/155 Mbit/s ATM-SDH/SONET FRAMER IC

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ABSTRACT:
A Node Network Interface/User Network Interface (NNI/UNI) ATM Framer ASIC which implements the SDH/SONET based Transmission Convergence (TC) sublayer of the B-ISDN reference model, has been fabricated. The FRAMER chip is suitable for 622.08 or 155.52 Mbit/s line rates. It incorporates 491K transistors, consumes 2W of power and has been implemented in 0.6μm CMOS technology.

1. INTRODUCTION

Asynchronous Transfer Mode (ATM) technology has been accepted as the major solution for the Broadband - Integrated Services Digital Network (B-ISDN) implementation. Synchronous Digital Hierarchy (SDH) and Synchronous Optical NETwork (SONET) are the most common transport network infrastructures, capable of carrying ATM cells among other types of communication traffic.

In this article we present the design and fabrication of the FRAMER ASIC prototype which implements the dual mode SDH/SONET based Transmission Convergence (TC) sublayer of the B-ISDN reference model, for 622.08 Mbit/s or 155.52 Mbit/s line rates. The FRAMER has been designed to serve as a generic building block for the B-ISDN either at the user network interface (UNI) to implement broadband terminal adaptors, or at the Node Network Interface (NNI) in the implementation of ATM switching systems. Its main task is the termination/generation of 622.08 Mbit/s (STM-4c/STS-12c) or 155.52 Mbit/s (STM-1/STS-3c) SDH or SONET frames carrying ATM cells. Fig. 1 shows that the FRAMER's positioning is in the physical (PHY) layer, lying between a high speed line tranceiver (PMD layer) and a Segmentation-And-Reassembly (SAR) Unit (ATM layer) [1], [2].

2. TRANSMITTER

Fig. 1 also shows FRAMER's internal architecture. In the transmit path, ATM cells from the SAR Unit are transferred to the 4-cell deep TxFIFO according to the 16-bit

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UTOPIA Interface specification [3]. The UTOPIA clock frequency in the TxFIFO and RxFIFO is in the 0-50 MHz range. ATM_Tx gets complete ATM cells stored in TxFIFO and overwrites each cell's HEC field with the internally generated CRC. Idle or unassigned cells are inserted when TxFIFO is empty. The payload of the continuous ATM cell stream is scrambled by a Self Synchronous Scrambler before passed to SDH_Framer.

The SDH_Framer maps ATM cells into the payload of STM-4c/STS-12c or STM-1/STS-3c frames. SDH or SONET format frames are composed in compliance with ITU-T [4], [5], [6], ATM Forum [7], and ANSI [8] specifications. The SDH_Framer does not simply insert a fixed value for H1 and H2 pointer bytes in the Tx frame (UNI usage), but it also enables the user to change the pointer with negative/positive justification and new-pointer commands, thus making FRAMER suitable for NNI usage as well. Among others, B1/B2/B3 parity bytes, Line FEBE, Path FEBE and alarm indicators, are generated and transmited in the Tx frame overhead. The Tx frame is scrambled by a Frame Synchronous Scrambler before passed octet-by-octet to the external line transmitter.

3. RECEIVER

In the receive path, SDH/SONET frames are passed octet-by-octet to the SDH_Deframer from the external line receiver. Since there is no information about byte and frame boundaries, SDH_Deframer performs byte and frame alignment. Moreover, pointer interpretation is performed according to the algorithm described in [4], [5]. SDH_Deframer descrambles the Rx frame, extracts and delivers ATM cells to ATM_Rx, extracts and processes frame overhead, calculates and verifies B1/B2/B3 parities, and generates useful alarm flags. ATM cells are received from the SDH_Deframer as a continuous byte stream with no information about the cell boundaries. ATM_Rx performs cell delineation according to [6] and simultaneously corrects possible single-bit errors in cell headers. Idle/unassigned cells are detected and discarded here. The valid information cells are farther passed for payload descrambling and afterwards are stored in the RxFIFO. Complete ATM cells in the 4-cell deep RxFIFO are transferred to the SAR Unit according to the 16-bit UTOPIA protocol.

4. MICROPROCESSOR INTERFACE

The μP_I/F is a powerful means for configuration, control, and status monitoring of the device. Initialization, programming of loopback-diagnostic modes, and operation mode selection (SDH or SONET, 622 or 155 Mbit/s) are some basic functions performed via μP_I/F. Furthermore, many different test scenarios can be applied through control registers (data corruption, B1/B2/B3 corruption, alarm insertion; enable-disable: scrambling, decrambling, HEC generation, single-bit correction, filtering of idle/unassigned cells etc) for self or system diagnostics. Moreover, useful reports for internal events during operation can be obtained through status registers (LOS, OOF, LOF, LOP, PAIS, LOC, LAIS, LFERF, PFERF, PRDI alarm flags, B1/B2/B3 errors, negative-positive justification, RxFIFO overrun, UTOPIA I/F errors etc). Via μP_I/F user has also access to statistics counters and overhead bytes of Rx and Tx frames.

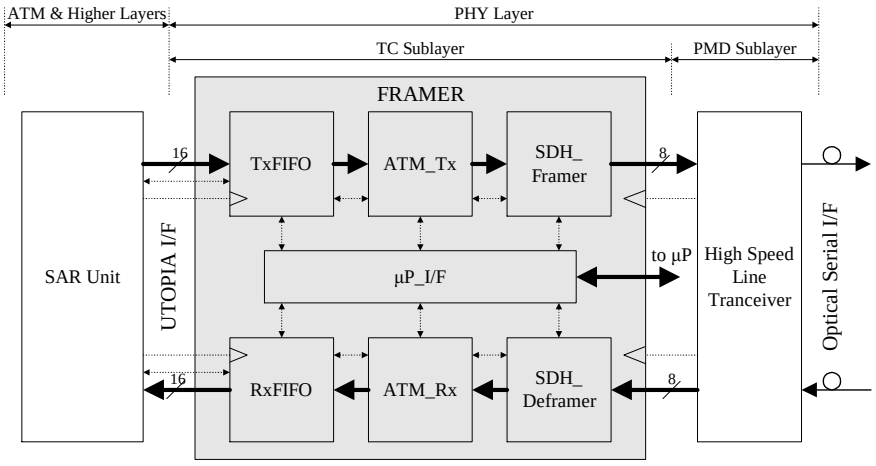

Fig. 1: System and FRAMER architecture

5. DESIGN ISSUES

The internal chip architecture uses 8-bit wide data paths clocked in 77.76 MHz for 622.08 Mbit/s operation. This relatively strict, for the 0.6μm technology, operating frequency, jointly with the complex functionality were the dominant factors for design decisions. Key issues for a successful design were the balance of the combinatorial delays between pipeline stages in the early VHDL-RTL level, the constraint driven logic optimization in SYNOPSYS Design Compiler (resulted to a high quality optimized netlist), and the decision to make hierarchical layout for increased locality of the interconnections and manageability. Global interconnect delays were kept low by careful floorplanning, as well as by the manual insertion of artificial super buffers built-up by parallel connection of simple buffers. Post-layout, back-annotated timing analysis reported a 9ns critical path.

Clock distribution was another important issue. Within each hierarchical block, the clock is distributed by a clock trunk, that being a distributed buffer assembled by several parallel buffers in the middle of the layout and connected with a couple of thick wires. This method ensures a very low clock skew within each block. For the inter-block skew, timing analysis with fine delay models was performed at the clock signals, and precise delays were placed in the layout to compensate the reported skew. An iterative procedure resulted to a very low skew (< 50 ps).

The storage unit of the FIFOs is a custom 4-port Static RAM which seats 4 ATM cells. The requirement of high fault coverage using a common scan style throughout the device, dictated the use of edge-triggered flip-flops as storage elements. To keep the FIFO's power consumption low, clock gating was used with the drawback of a complexity increase. Fig. 2 shows a microphotograph of the die. The basic features of the FRAMER are summarized in Table 1.

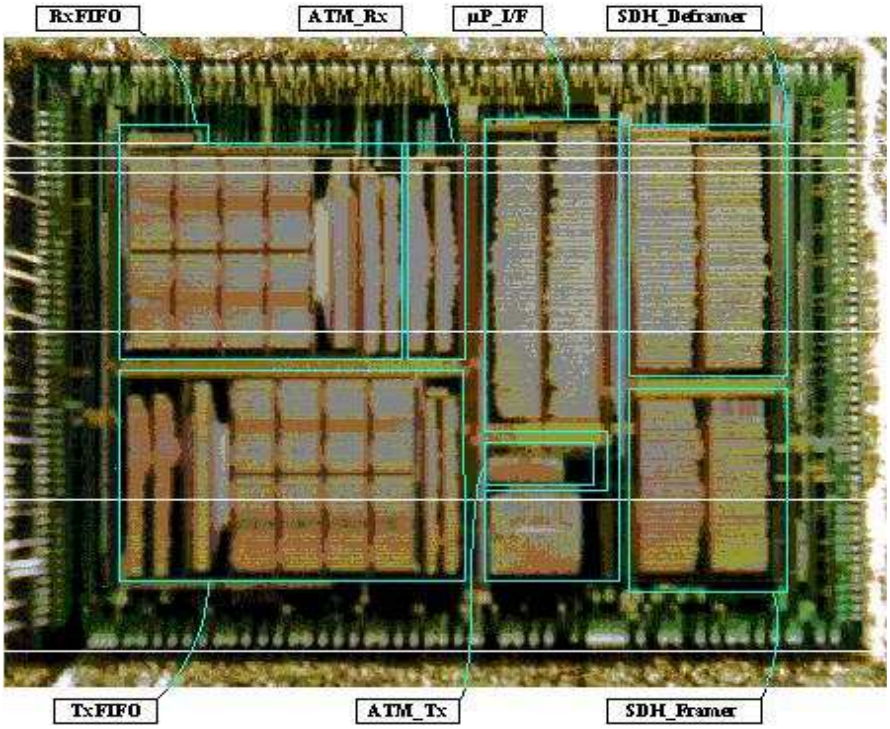

Fig. 2: Chip Microphotograph

Fig. 3: Test Bench Board

Table 1: *Summary of FRAMER Features*

Link Speed	622.08 or 155.52 Mbit/s (77.76/19.44 MHz x 8 parallel)
Technology	0.6μm Double-Metal CMOS
Operating Frequency	Internal Logic & Line I/F: 77.76 MHz UTOPIA I/F: 0-50 MHz
FIFO Buffers	2 FIFO buffers, 4 ATM cell each
Transistor Count	491K
Supply Voltage	+5V
Die Size	13.54mm x 10.36mm = 140mm^2
Power Consumption	2W @ 77.76MHz
Package	208-pin PQFP

For manufacturing testing, we used full internal scan strategy and an ATPG tool achieved 97% fault coverage. Moreover, for boundary scan a standard 5-signal JTAG interface is provided.

For the purposes of functional testing a flexible test bench using reconfigurable logic was developed. The FRAMER's built-in control and status monitoring registers facilitated the application of many test scenarios such as loopback-diagnostic modes and board-to-board communication and verified the proper device operation for internal clock frequencies up to 110MHz. Fig. 3 shows the test bench board.

6. CONCLUSIONS

It was fabricated a 622 Mbit/s ATM-over-SDH physical layer ASIC using a 0.6μm CMOS technology. The main task of the FRAMER is the termination/generation of 622.08 Mbit/s (STM-4c/STS-12c) or 155.52 Mbit/s (STM-1/STS-3c) SDH or SONET frames carrying ATM cells, and can serve as a generic building block in the UNI/NNI of B-ISDN networks. The die-area is 140mm^2 incorporating 491K transistors. The chip was tested to operate correctly up to rates of 880 Mbit/s.

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